R E M A R K S

Careful review and examination of the subject application are noted and appreciated. The following remarks refer to the Office Action mailed November 18, 2003.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments can be found in the specification, for example, on page 6 lines 12-18, page 9 lines 2-3 and FIGS. 2 and 4 as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 2, 4, 6, 7, 9, 13, 16, 21 and 22 under 35 U.S.C. §102(b) as being anticipated by Uchida et al. '304 (hereafter Uchida) has been obviated by appropriate amendment and should be withdrawn.

Uchida concerns a semiconductor integrated circuit (Title). Uchida does not appear to disclose or suggest every element as arranged in the claims. Anticipation requires the presence in a single prior art reference disclosure of **each and every element** of the claimed invention, **arranged as in the claim** (Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)(Emphasis added).

As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 1 provides an input pin for data and a shift register couplable to the input pin for shifting in the data. In contrast, Uchida appears to be silent regarding a bonding pad 10 being couplable to the ID code register 5 for shifting in data. In particular, FIGS. 1, 2, 5, 6, 7 and 8 of Uchida only show the bonding pad 10 connected to the multiplexers 41, 42 and 43 within an ID code setting portion 4. The rest of Uchida appears to be silent regarding the bonding pad 10 being couplable to the ID code register 5. Therefore, Uchida does not appear to disclose or suggest an input pin for data and a shift register couplable to the input pin for shifting in the data as presently claimed. Claims 13 and 14 provide language similar to claim 1. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 2 provides that the configuration signals are user variable. In contrast, column 10, lines 39-41 of Uchida disclose that ID code is determined in an assembly process and thus is **fixed**. Simply because pads 12 and 13 of Uchida are labeled "input" does not expressly or inherently disclose variability by a user. Therefore, Uchida does not appear to disclose or suggest configuration signals that are user variable as presently claimed. Claim 15 provides language similar to claim 2. As such, claims 2

and 15 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 4 provides that each value of a device identification identifies a unique configuration of a circuit. In contrast, Uchida appears to be silent regarding the IC chip 1 having a unique configuration determined from the pads 12 and 13. In particular, none of the figures in Uchida show any connection between the function circuit portion and pad 12 or pad 13. Therefore, Uchida does not appear to disclose or suggest that each value of a device identification identifies a unique configuration of a circuit as presently claimed. claim 16 provides language similar to claim 4. As such, claims 4 and 15 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 6 provides a second logic gate configured to generate a second identification signal from said configuration signals. In contrast, Uchida appears to be silent regarding a second logic gate receiving both signals from pads 12 and 13. The argument on page 3, paragraph 6 of the Office Action is irrelevant as "the input B" of element 37 from Uchida does not generate a second identification signal **from both signals** from pads 12 and 13. Therefore, Uchida does not appear to disclose or suggest a second logic gate configured to generate a second identification signal from said configuration signals as presently claimed.

The assertion on page 3, paragraph 6 of the Office Action that logic gates are inherent to decoders is respectfully traversed. Inherency requires certainty of results, not mere possibility. See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981). Since the decoder 37 could be implemented by connecting two of the outputs to input A and the other two outputs to input B, no logic gates are necessary and thus are not inherent. As such, claim 6 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 9 provides a FIFO memory and (from claim 1) a shift register. In contrast, Uchida appears to be silent regarding both a FIFO memory and a shift register. Furthermore, the assertion on page 3, paragraph 7 of the Office Action that the claimed FIFO is similar to the ID code register 5 of Uchida conflicts with the assertion on page 2, paragraph 3 of the Office Action that the ID code register 5 of Uchida is similar to the claimed shift register. The single ID code register 5 of Uchida cannot simultaneously anticipate two claim elements under *Lindemann Maschinenfabrik GmbH*. Therefore, Uchida does not appear to disclose or suggest at least one of (i) a FIFO memory and (ii) a shift register as presently claimed. As such, claim 9 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 21 provides an output multiplexer configured to multiplex a device identification from a shift register to an output pin and (from claim 1) a first multiplexer. In contrast, Uchida appears to be silent regarding an output multiplexer. Furthermore, the assertion on page 5, paragraph 13 that the ID code setting portion 4 of Uchida is similar to the claimed output multiplexer conflicts with the assertion on page 2, paragraph 3 that the multiplexers 41, 42 or 43 within the ID code setting portion 4 are similar to the claimed first multiplexer. Therefore, Uchida does not appear to disclose or suggest at least one of (i) an output multiplexer configured to multiplex a device identification from a shift register to an output pin and (ii) a first multiplexer as presently claimed. Claim 22 provides language similar to claim 21. As such, claims 21 and 22 are fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 3, 10, 12, 18 and 20 under 35 U.S.C. §103(a) as being unpatentable over Uchida in view of the Background section of the pending application is respectfully traversed and should be withdrawn.

The rejection of claim 8 under 35 U.S.C. §103(a) as being unpatentable over Uchida in view of Gates '207 has been obviated by

appropriate amendment and should be withdrawn. Claim 8 has been canceled.

The rejection of claims 5 and 17 under 35 U.S.C. §103(a) as being unpatentable over Uchida in view of Adams et al. '732 (hereinafter Adams) is respectfully traversed and should be withdrawn.

Uchida concerns a semiconductor integrated circuit (Title). Gates concerns a method and apparatus for automatically loading configuration data on reset into a host adapter integrated circuit (Title). Adams concerns a storage device capacity management (Title). Uchida, Gates, Adams and the Background Section of the application, alone or in combination, do not appear to teach or suggest every claimed element. Furthermore, *prima facie* obviousness has not been established for lack of evidence of motivation to combine the references and reasonable expectation of success.

"[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicants."[1] "[T]he factual inquiry whether to combine references must be thorough and

---

[1] *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citing *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

searching."[2] "This factual question ... [cannot] be resolved on subjective belief and unknown authority."[3] "It must be based on objective evidence of record."[4] The Examiner must show that (a) there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (b) there is a reasonable expectation of success, and (c) the prior art reference (or combination of references) teaches or suggests all of the claim limitations as arranged in the claims.[5] Furthermore, The Court of Appeals for the Federal Circuit has indicated that the requirement for showing the teaching of motivation to combine references is "rigorous" and must be "clear and particular".[6]

Claim 3 provides that the circuit comprises a JTAG compliant controller. In contrast, page 5, paragraph 16 of the Office Action admits that Uchida does not disclose a JTAG compliant controller. The Background Section of the application is also silent regarding a JTAG compliant controller. Therefore, Uchida

---

[2] *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001).

[3] *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

[4] *Id.* at 1343, 61 USPQ2d at 1434.

[5] Manual of Patent Examining Procedure (M.P.E.P.), Eighth Edition, Revised February 2003, §2142.

[6] *In re Anita Dembiczak* and *Benson Zinbarg*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999)

and the Background Section of the application, alone or in combination, do not appear to teach or suggest a JTAG compliant controller as presently claimed.

Furthermore, the asserted motivation on page 5, paragraph 16 of the Office Action to combine Uchida with the Background Section does not appear to be based on either Uchida, the Background Section or knowledge generally available to one of ordinary skill in the art. Therefore, the asserted motivation in the Office Action appears to be merely a conclusory statement. The fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness (MPEP §2143.01). In addition, no evidence is provided in the Office Action for a reasonable expectation of success. Furthermore, no admission has been made that the Background Section of the application qualifies as prior art under 35 U.S.C. §102/§103. Therefore, *prima facie* obviousness has not been established. As such, claim 3 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 5 provides that a device identification determines a storage capacity of a circuit. In contrast, page 7, paragraph 20 of the Office Action admits that Uchida does not disclose a device identification determining a storage capacity of a circuit. Furthermore, Adams appears to be silent regarding a device identification determining a storage capacity of a circuit. In particular, lines 10-11 of the Abstract of Adams state that

identification information is for "uniquely identifying the memory device." Furthermore, lines 1-3 of the Abstract of Adams state that the storage medium is of "a predetermined size and corresponding capacity." Adams appears to be silent that the predetermined storage capacity is somehow variable or that the capacity is somehow governed by the device identification. Therefore, Uchida and Adams, alone or in combination, do not appear to teach or suggest a device identification that determines a storage capacity of a circuit as presently claimed.

Furthermore, nowhere in the Abstract does Adams appears to state that the invention of Adams would improve control over device configuration as asserted on page 7, paragraph 20 of the Office Action. Therefore, the asserted motivation appears to be merely conclusory. The Office Action is also silent regarding any evidence for a reasonable expectation of modifying the IC Chip 1 of Uchida to manage RAM capacity using techniques developed by Adams for a host system managing a hard disk drive. Therefore, *prima facie* obviousness has not been established. Claim 17 provides language similar to claim 5. As such, claims 5 and 17 are fully patentable over the cited reference and the rejection should be withdrawn.

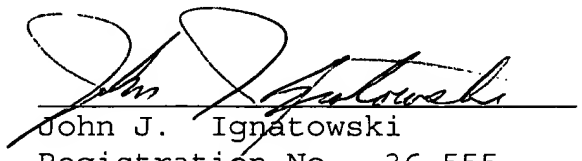
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



John J. Ignatowski
Registration No. 36,555
24025 Greater Mack, Suite 200
St. Clair Shores, MI 48080
(586) 498-0670

Dated: February 18, 2004

Docket No.: 0325.00374